WHAT IS CLAIMED IS:

1. A method for storing and retrieving image information stored in a dual-ported memory, the method comprising:

providing a memory comprising a matrix of memory cells that are addressable in orthogonal directions;

receiving image information for storage in the memory, said image information comprising a plurality of data words;

storing said image information in the memory by storing each data word of the image information in a row of the matrix; and

retrieving individual bit planes of the image information from the memory by retrieving individual columns of bits from the corresponding columns of the matrix.

2. The method of claim 1, wherein said orthogonal directions comprise a horizontal direction and a vertical direction.

3. The method of claim 1, wherein said memory is addressable via orthogonally-connected address buses.

4. The method of claim 1, wherein said image information comprises pixel values.

5. The method of claim 1, wherein said memory comprises static random access memory (SRAM).

6. The method of claim 1, wherein each said data word comprises a pixel value of a particular bit width.

7. The method claim 6, wherein said bit width is equal to at least 16 bits.

8. The method claim 1, wherein said step of storing said image includes:

storing said image information in the memory by storing successive data words of the image information in successive rows of the matrix.

9. The method of claim 1, wherein the most significant bits (MSBs) of the data words are stored on one side of the matrix, with the least significant bits (LSBs) of the data words being stored on an opposing side of the matrix.

10. The method claim 1, wherein said step of retrieving individual bit planes comprises:

retrieving bits from successive columns of the matrix.

11. The method claim 10, wherein bits are first retrieved from columns of the matrix storing the most significant bits (MSBs) of the data words.

12. The method of claim 1, wherein each said data words stored in memory is converted from 2's complement representation to a sign plus magnitude representation.

13. The method of claim 1, wherein said step of retrieving individual bit planes includes:

retrieving bits by starting with a column of most significant bits, then retrieving columns of lesser-significant bits.

14. The method claim 1, wherein said data words are stored in a manner supporting little-endian format.

15. The method of claim 1, wherein said data words are stored in a manner supporting big-endian format.

16. An orthogonal memory device comprising:

data inputs;

an array of storage elements for bit storage of information arriving from said data inputs;

an address decoding mechanism for selecting a particular row or column of storage elements, said address decoding mechanism supporting read access in a direction that is orthogonal to that for write access; and

data outputs to output data read from said storage elements.

17. The device of claim 16, wherein each storage element comprises a flip-flop.

18. The device of claim 16, wherein said array comprises a two-dimensional array of storage elements.

19. The device of claim 18, wherein said two-dimensional array is asymmetrical, such that the bit width of said two-dimensional array in one direction is not equal to the bit width of said two-dimensional array in another, orthogonal direction.

20. The device of claim 18, wherein said two-dimensional array is symmetrical, such that the bit width of said two-dimensional array in one direction is equal to the bit width of said two-dimensional array in another, orthogonal direction.

21. The device of claim 16, wherein read access occurs in a horizontal direction of the array.

22. The device of claim 16, wherein read access occurs in a vertical direction of the array.

23. The device of claim 16, wherein write access occurs in a horizontal direction of the array.

24. The device of claim 16, wherein write access occurs in a vertical direction of the array.

25. The device of claim 16, wherein said array has a bit width of at least 4 bits.

26. The device of claim 16, wherein said array has a bit width selected from between 4 bits to 128 bits.

27. The device of claim 16, wherein said data inputs comprises a port.

28. The device of claim 16, wherein said data inputs comprises a bus.

29. The device of claim 16, wherein said data outputs comprises a port.

30. The device of claim 16, wherein said data outputs comprises a bus.

31. The device of claim 16, wherein said data inputs and said data outputs share a common bus.

32. The device of claim 16, wherein said data inputs and said data outputs each employ a separate bus.

33. The device of claim 16, wherein said data inputs provide sequential pixel value information from a digital image.

34. The device of claim 16, wherein said data inputs provide non-sequential pixel value information from a digital image.

35. The device of claim 16, wherein said data inputs provide input originally in 2's complement format.

36. The device of claim 16, wherein inputs are converted to 1's complement format for storage.

37. The device of claim 16, wherein outputs are provided in 2's complement format.